



# PROJECT DELIVERABLE REPORT

## INTEL-LINE

### Work Package 5

### Deliverable 5.2

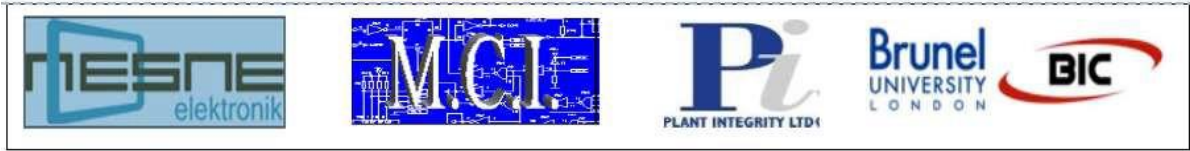
## Personnel Training Certification

**Due date of deliverable: 31<sup>st</sup> July 2019**  
**Actual submission date: 28<sup>th</sup> September 2019**

**Authors:**  
**PLANT INTEGRITY, BRUNEL UNIVERSITY**

**Dissemination Level: Public**

<b>Project Call:</b>	Fast Track to Innovation Pilot
<b>Project Number:</b>	720402
<b>Project Start Date:</b>	01 October 2016
<b>Project's coordinator:</b>	Mrs Hilal Tolasa Gundogdu (Nesne electronic)
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<b>E-mail:</b>	<a href="mailto:hilalt@nesne.com">hilalt@nesne.com</a>



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An intelligent inspection system  
for improved and efficient power line cable maintenance  
[www.intel-line.eu](http://www.intel-line.eu)

### **Summary for the Personnel Training Certification**

The Intel-line training materials (D3.3) were presented at the system demonstration held on 9<sup>th</sup> April 2019 for RTE and held on 1<sup>st</sup> July 2019 for BORUSAN.

Each member of the Intel-line consortium attended at least one of these demonstrations.

On the top of these demonstrations, a refresher course was organized (via conference call) for the attention of the Intel-line consortium only. This training course was organised to allow members of the Intel-line consortium to gain a deeper understanding of the Intel-line technology and operating system.

The training record below certifies that the Intel-line consortium attended the training courses.



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### Training Record Sheet

Training Package Title: Training course for the Intel-line technology and system

Tutor Company: Plant Integrity  
Brunel University

Date of Training: 9<sup>th</sup> April, 1<sup>st</sup> July and 11<sup>th</sup> July 2019

Location of Training: TWI, Granta Park, Great Abington. Cambridge, CB21 6AL  
and Conference call

#### Attendance Record:

Name	Company	Job Title
Hilal Tolasa Gündoğdu	NESNE Electronic	Executive Director
Ayca Pinar Akdurak Bal	NESNE Electronic	Project Manager
Pierre-Olivier Jost	MCI Electronics	Scientific Project Manager
Julien Jost	MCI Electronics	Technical Project Manager
Jean-Claude Tillet	MCI Electronics	Ingenieur R&D
Nicolas Trenado	MCI Electronics	Responsable Études, R&D and Innovation

The above Training Package has been delivered and both Plant Integrity and Brunel University are satisfied that the objectives of the training have been achieved.

Date: 02<sup>nd</sup> September 2019

# INTEL-LINE EXAM PAPER

## MULTIPLE CHOICES

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### Appendix A - Exam paper

**Name** : Ayca Pinar Akdurak Bal

**Company** : Nesne Electronic

**Date** : 11<sup>th</sup> July 2019

**Exam location:** Conference call

Q1: What non-homogeneous conductors the Intel-Line system has been designed for?

- ACAR (Aluminium Conductor Alloy Reinforced)
- ACSR (Aluminium Conductor Steel Reinforced)
- ACSS (Aluminium Conductor Steel Supported)
- AACSR (Aluminium Alloy Conductor Steel Reinforced)

Q2: What maximum voltage can the Intel-Line system operate at?

- 30 KV
- 138 KV
- 220 KV
- 400 KV

Q3: How many transducers does the Intel-Line collar hold?

- 4
- 6
- 8
- 10

Q4: What are the width of the transducers used in the Intel-line collars?

- 3 and 5 mm

# INTEL-LINE EXAM PAPER

## MULTIPLE CHOICES

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- 5 and 7 mm
- 5 and 13 mm
- 7 and 13 mm

Q5: In the Intel-Line collars, what is the maximum force applied to the transducer?

- 50N
- 100N
- 150N
- 200N

Q6: What cables is the Intel-Line system primary designed for?

- Squirrel and Fox
- Cat and Rabbit
- Dog and Bear
- Lion and Tiger

Q7: What is the frequency range for Guided Wave Testing?

- 0 – 20 Hz
- 20 Hz – 20 kHz
- 20 kHz – 500 kHz
- 20 kHz – 1 GHz

Q8: What is the frequency of interest in multi-wires?

- 20 kHz – 200 kHz
- 20 kHz – 300 kHz
- 20 kHz – 400 kHz
- 20 kHz – 500 kHz

# INTEL-LINE EXAM PAPER

## MULTIPLE CHOICES

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Q9: How many channels are active in the Intel-Line Hardware?

2

4

6

8

Q10: What is the maximum signal output voltage of the hardware?

100 Vpp

200 Vpp

300 Vpp

400 Vpp

Q11: What is the usual number of wave cycles used for data collection?

3

5

7

9

Q12: What is the "Accumulate" value used for data collection?

64

128

256

512

Q13: Out of 100, what is the scale of the transmitted amplitude for data collection?

# INTEL-LINE EXAM PAPER

## MULTIPLE CHOICES

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- 0
- 40
- 70
- 100

Q14: Which value is the Rx Gain usually set at?

- 8
- 16
- 32
- 64

Q15: What point "value" does the Acquisition Start?

- 0
- 1
- 2
- 3

Q16: What is the first step in the data collection process?

- Set Wave Parameters
- Start Fire
- Start Recording
- Start Range Fire

Q17: For a Sweep Function Wave type, what values are the Tx Samples set at?

- 5 or 10
- 50 or 100



# INTEL-LINE EXAM PAPER

## MULTIPLE CHOICES

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500 or 1000

5000 or 10000

Q18: For a Sweep Function Wave type, what value is the Tukey Ratio set at?

0

1

2

3

# INTEL-LINE EXAM PAPER

## MULTIPLE CHOICES

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### Appendix B - Exam paper

**Name** : Hilal Tolasa Gundogdu

**Company** : Nesne Electronic

**Date** : 9th of April and 11<sup>th</sup> July 2019

**Exam location:** TWI, Granta Park, Great Abington. Cambridge, CB21 6AL

and Conference call

Q1: What non-homogeneous conductors the Intel-Line system has been designed for?

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3 and 5 mm

5 and 7 mm

5 and 13 mm

7 and 13 mm

# INTEL-LINE EXAM PAPER

## MULTIPLE CHOICES

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- 20 kHz – 300 kHz
- 20 kHz – 400 kHz
- 20 kHz – 500 kHz

Q9: How many channels are active in the Intel-Line Hardware?

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- 4
- 6
- 8

Q10: What is the maximum signal output voltage of the hardware?

- 100 Vpp
- 200 Vpp

# INTEL-LINE EXAM PAPER

## MULTIPLE CHOICES

---

300 Vpp

400 Vpp

Q11: What is the usual number of wave cycles used for data collection?

3

5

7

9

Q12: What is the "Accumulate" value used for data collection?

64

128

256

512

Q13: Out of 100, what is the scale of the transmitted amplitude for data collection?

0

40

70

100

Q14: Which value is the Rx Gain usually set at?

8

16

32

64

Q15: What point "value" does the Acquisition Start?

0

1

2

3

Q16: What is the first step in the data collection process?

# INTEL-LINE EXAM PAPER

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